Knowledge Sharing Centre

Manufacturing Technology Conference 2023

ASML Defectivity and Contamination Control

Defectivity and Contamination Control

The importance for ASML and why processes at suppliers matter

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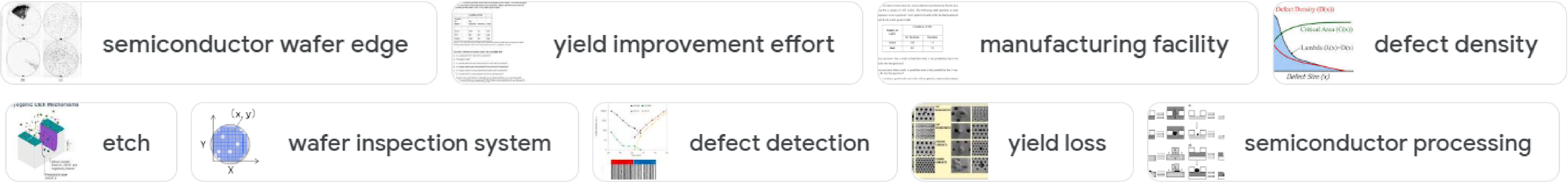
Business drivers for defectivity & contamination control

2023

Business drivers for defectivity & contamination control



+ 37.000.000 hits in google when looking for:
"semiconductor defectivity yield particle "

Primary (direct) driver:

Yield and Device performance:

- Particles on reticle and wafer ~ Printed defects ~ Yield
- Wafer & reticle backside particles ~ Overlay & focus error ~ Device performance & Yield

Indirect driver:

Availability (in VHV cycle time) & reliability

- Cleaning actions ~ System down time ~ Availability
- Particle event ~ Root cause finding ~ Availability / Reliability
- Guarantee lifetime (mechanical part failure) ~ Down time ~ Availability / Reliability

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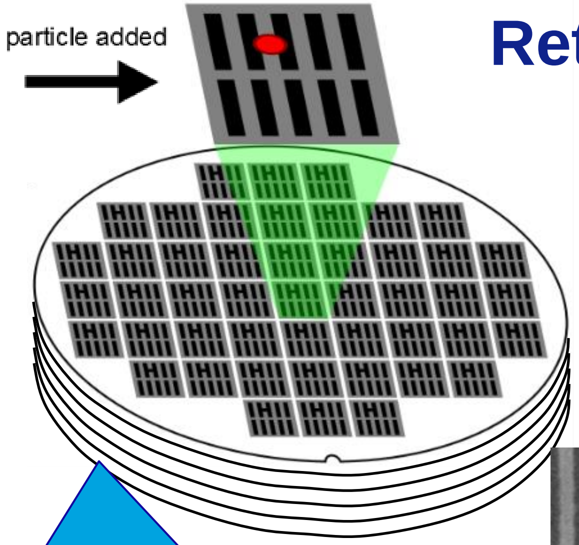
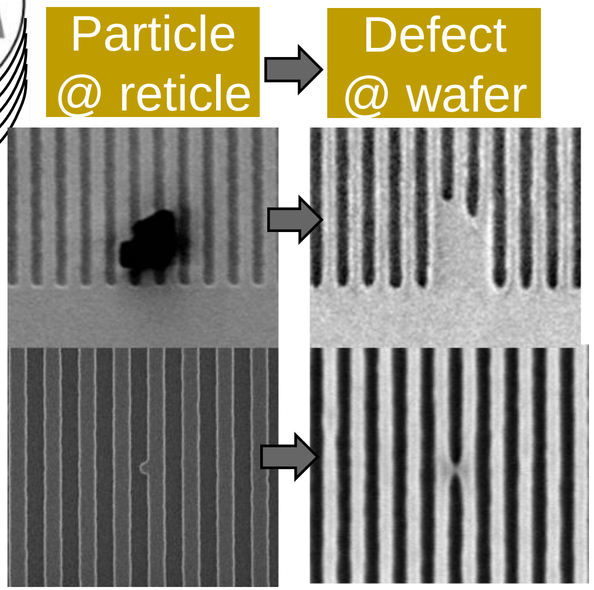
Particle contamination control = Defectivity

focusing on reticle and wafer frontside defectivity;

Reticle

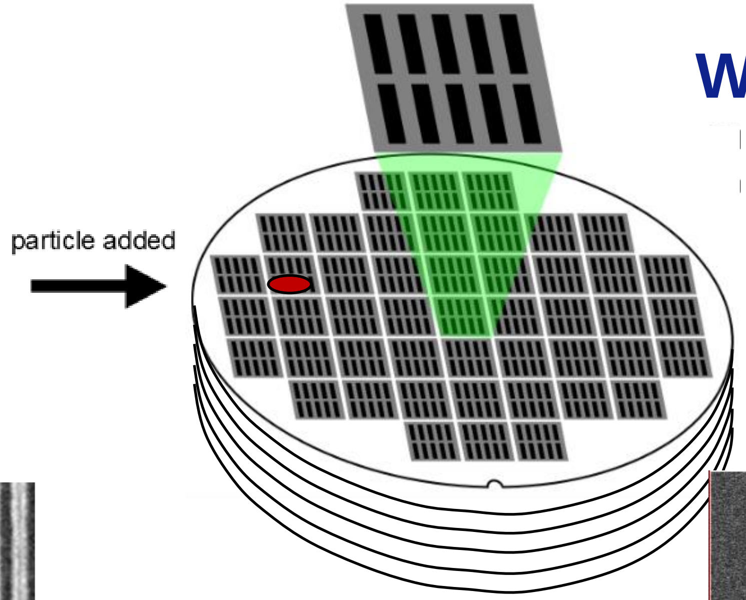


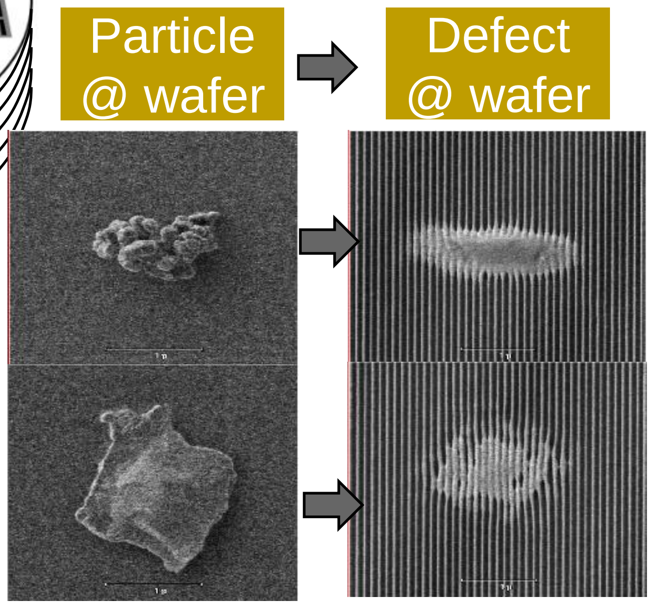
Note within DUV a pellicle is used to mitigate particle contamination
EUV has w/wo pellicle strategy due to productivity loss of pellicle



Particle on reticle front side <u>repeats</u> for each die on wafer (100% yield loss for full field dies);

Wafer





Particle on wafer front side kills one die, die is fully processed providing no value for the customer;

Example: value wafer defectivity

A wafer contains about 450 dies; loosing 1 die due to a defect represents ~ 33 € customer value loss per wafer

- Assume 6 dies per image on a 300mm wafer with 76 images

  ~ 450 dies per wafer exposed (= (76×6))

- Assume 15000 €/wfr customer value (see table below)

  Loosing 1 die on a wafer represents 33 € customer value (15000 €/wfr / 450)

https://www.tomshardware.com/news/tsmcs-wafer-prices-revealed-300mm-wafer-at-5nm-is-nearly-dollar17000

Table 9: Calculation of foundry sale price per chip in 2020 by node

Line	Node (nm)	90	65	40	28	20	16/12	10	7	5
1	Mass production year and quarter[220]	2004 Q4	2006 Q4	2009 Q1	2011 Q4	2014 Q3	2015 Q3	2017 Q2	2018 Q3	2020 Q1
2	Capital investment per wafer processed per year	$4,649	$5,456	$6,404	$8,144	$10,356	$11,220	$13,169	$14,267	$16,746
3	Net capital depreciation at start of 2020 (25.29% / year)	65%	65%	65%	65%	65%	65%	55.1%	35.4%	0.0%
4	Undepreciated capital per wafer processed per year (remaining value at start of 2020)	$1,627	$1,910	$2,241	$2,850	$3,625	$3,927	$5,907	$9,213	$16,746
5	Capital consumed per wafer processed in 2020	$411	$483	$567	$721	$917	$993	$1,494	$2,330	$4,235
6	Other costs and markup per wafer	$1,293	$1,454	$1,707	$2,171	$2,760	$2,990	$4,498	$7,016	$12,753
7	Foundry sale price per wafer	$1,650	$1,937	$2,274	$2,891	$3,677	$3,984	$5,992	$9,346	$16,988
8	Foundry sale price per chip	$2,433	$1,428	$713	$453	$399	$331	$274	$233	$238

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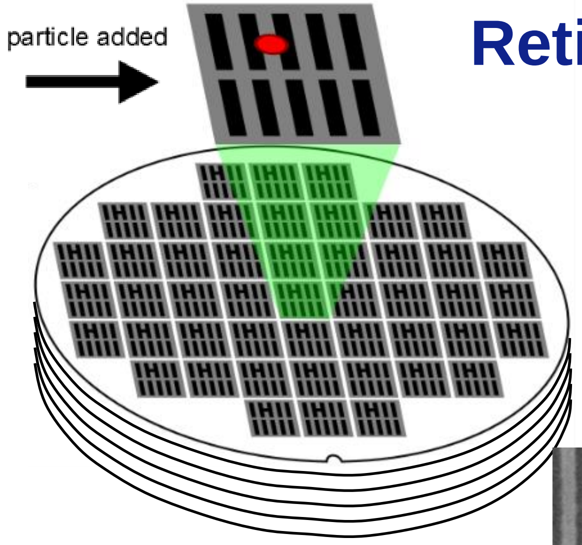
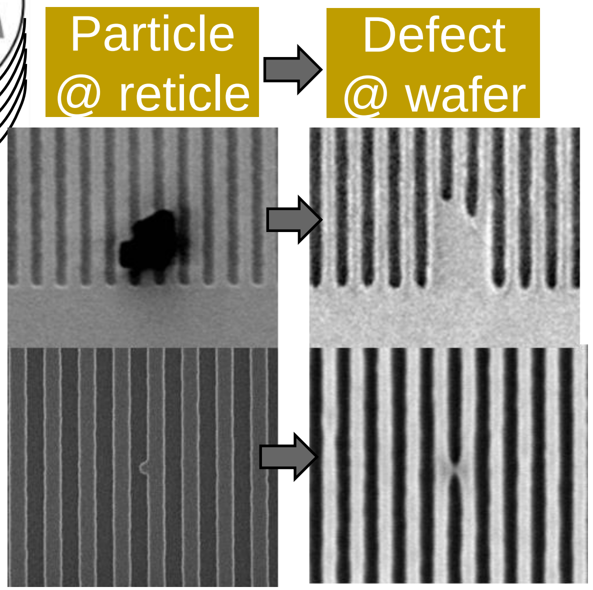
Critical defect size for reticle and wafer defectivity

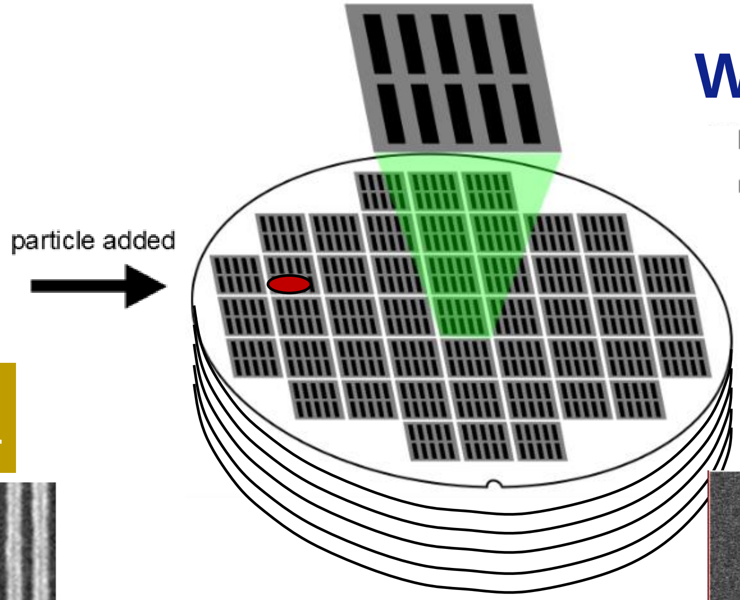
Reticle

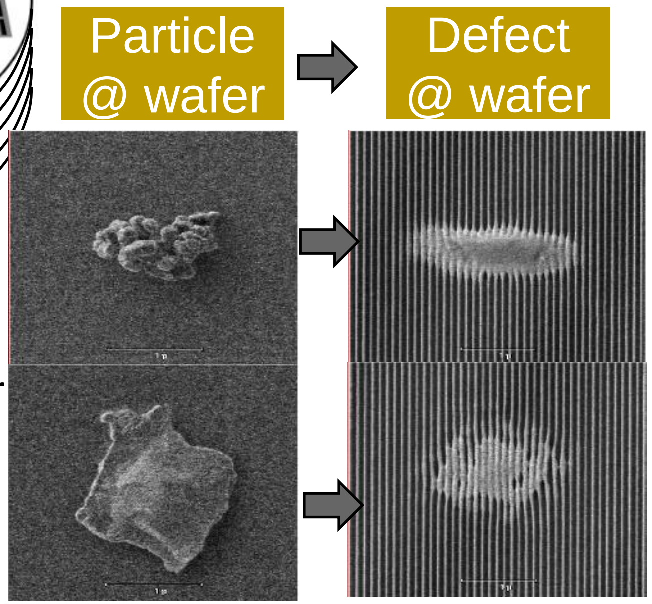




Damage threshold for future ASML system is **~32nm** @ reticle

Wafer

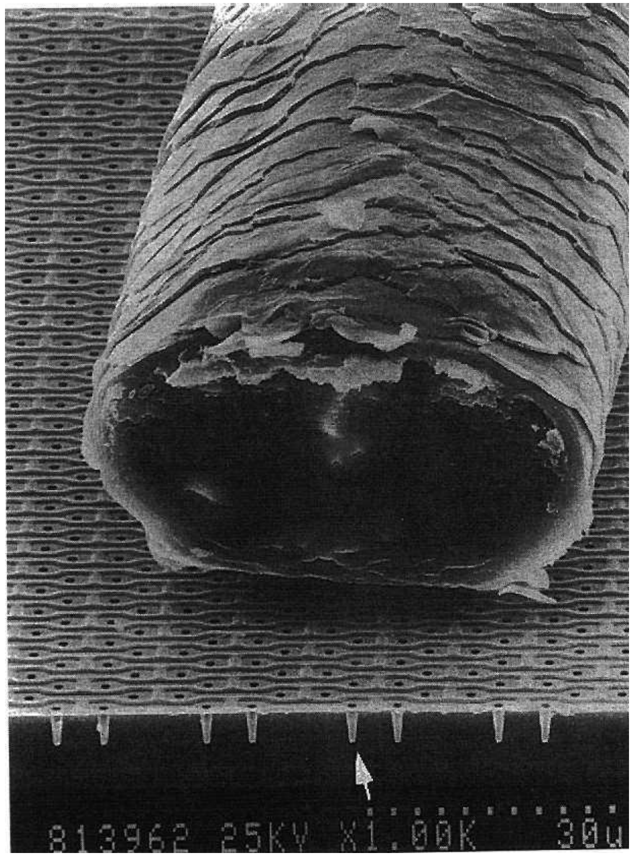




Damage threshold for future ASML system is **~ 4nm** @ wafer

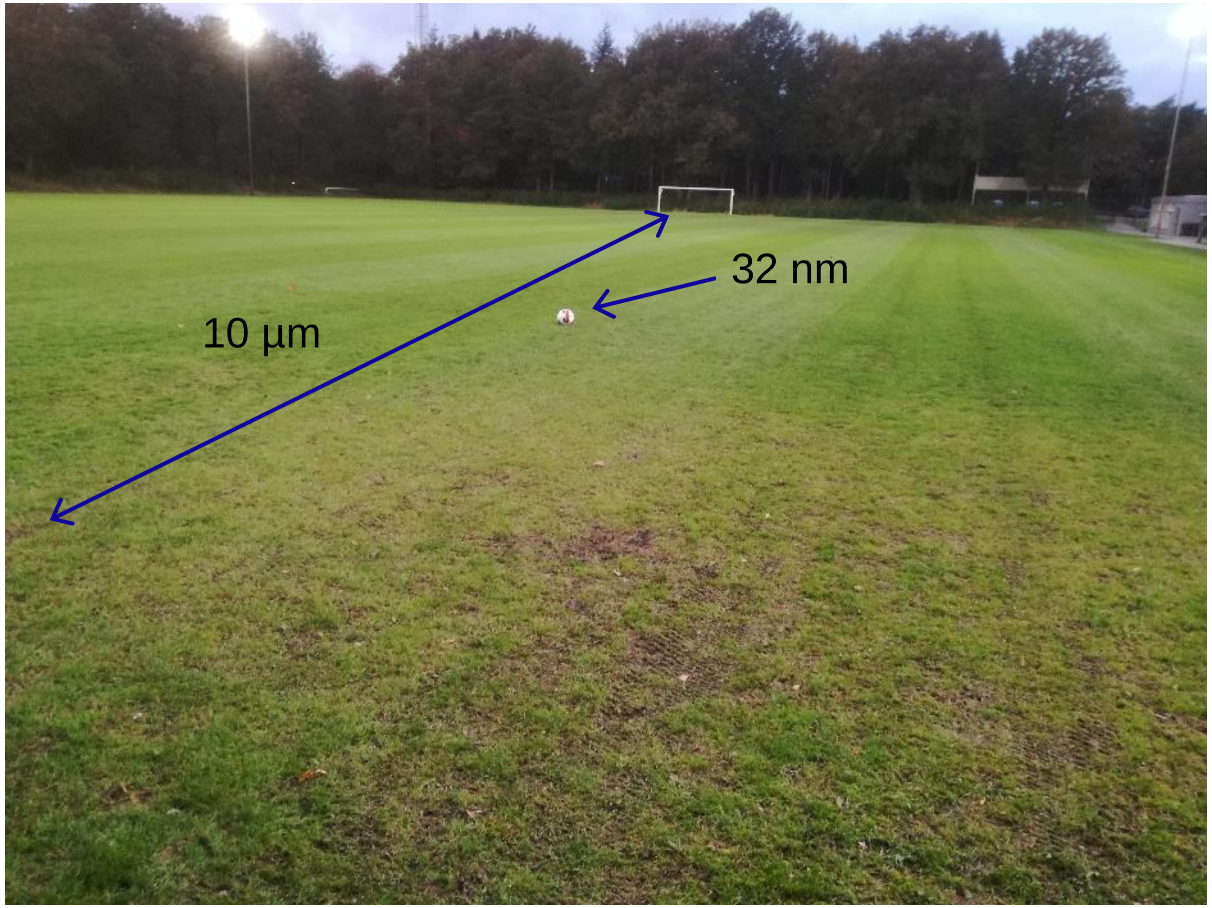
How to put 32nm and 4nm critical particle size in perspective?

A human hair ~ 50 - 100 µm
on 300 nm technology



Source: Siemens AG (Infinion)

Imagine the size of a football field to be 10 um
than the football would represent about 30nm



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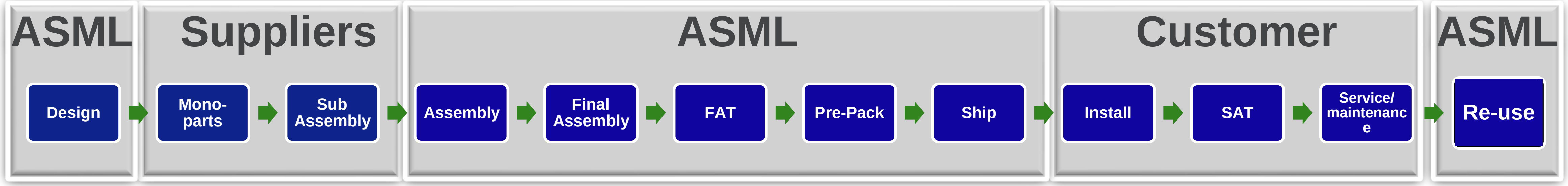
Contamination Control Approach for new EUV tool

Implement lessons learned

- Secure cleanliness and defectivity performance by design
- Parts cleanliness and defectivity control over entire product lifecycle



FAT: Factory Acceptance Test; SAT: Site Acceptance Test

Defectivity:

Finding and understanding the root cause (mechanisms) of particles on wafers and reticles (defectivity chain) and translating this understanding in design solutions and design rules for future systems

Contamination control:

Understanding processes and external aspects that contribute to part, module and system cleanliness (e.g. cleanroom, design and manufacturing for cleanliness, shipping, storage and handling processes, scanner integration, maintenance and service)

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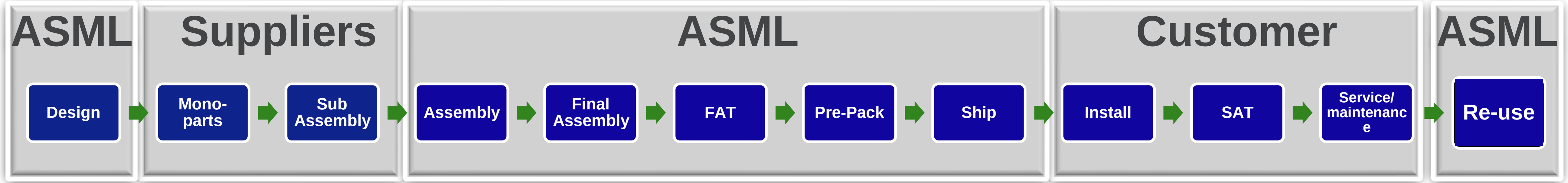
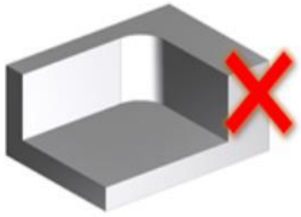
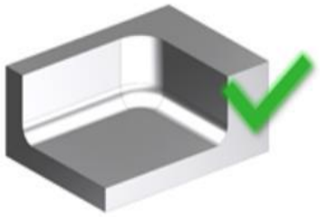
Contamination Control Management Strategy

Improve design, manufacturing and assembly processes

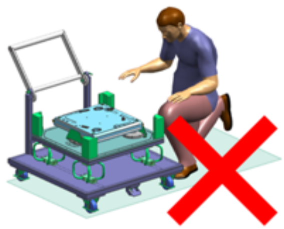


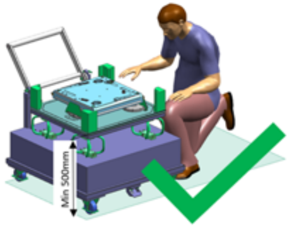
- By design
  - **Design rules:**
    - Introduction cleanliness grades
      - → Limiting acceptable number of particles on surface
    - Improved cleanability of parts / assy
      - → Limit use sharp edges, number of pockets, minimize topography….
  - **Review the design with the focus on defectivity impact**
    - Dedicated defectivity FMEA's





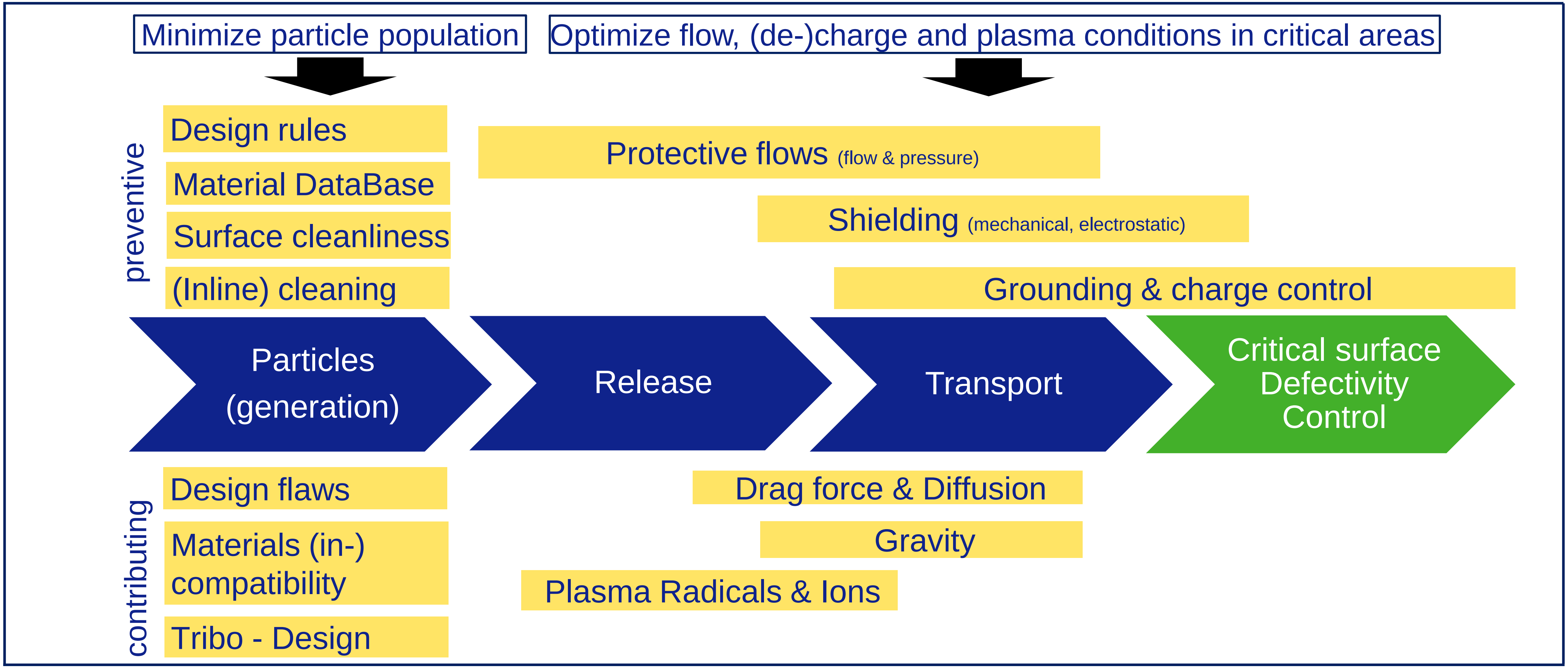
- By manufacturing
  - **Cleaning capability for critical parts**
  - **Introduce clean way of working**
    - Set of trainings available for supplier to understand the basics of clean manufacturing
    - Share does/don't, how to handle, store, transport, etc..
    - Inform about forbidden manufacturing processes
  - **Review manufacturing process as proposed by supplier**
    - Dedicated defectivity manufacturing process FMEA's
    - Audit manufacturing capabilities and propose improvements
  - **Team in place to support most critical part suppliers.**





Defectivity Management Strategy

Break all possible links in the defectivity chain using ASML standards, (NXE) learnings, design rules and proven defectivity control principles



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Contamination Control Management Strategy

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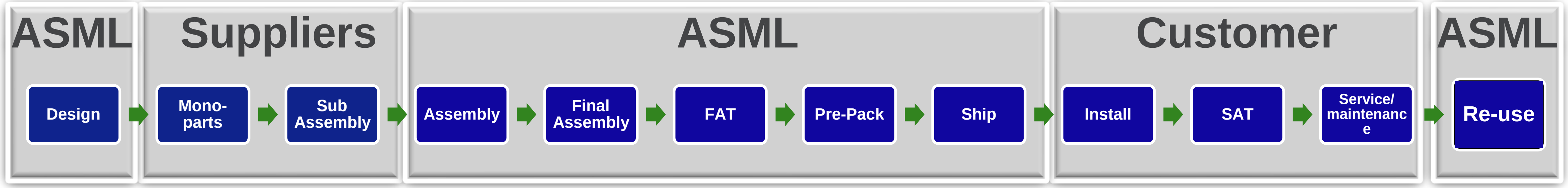

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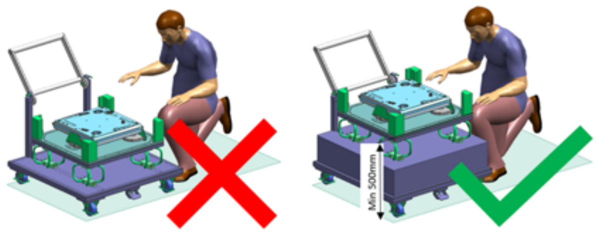

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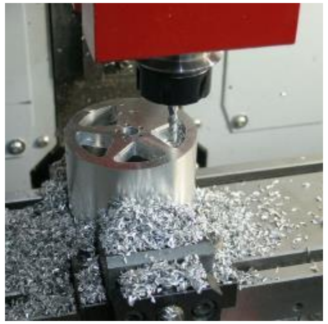
How to get critical (grade 1) mono parts clean

an analogy

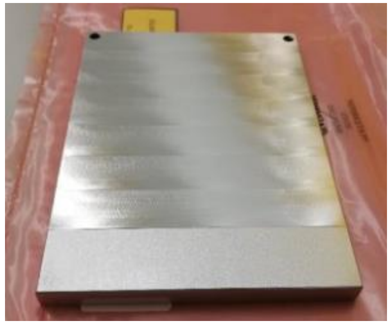


Parts contaminated from manufacturing

=

Cleaning Service Providers (CSP)

=



Grade 1 parts ready for integration

=

Dirty dishes

Dishwasher

Clean dishes

ASML two-step approach for clean mono parts

Step 1: CSP release

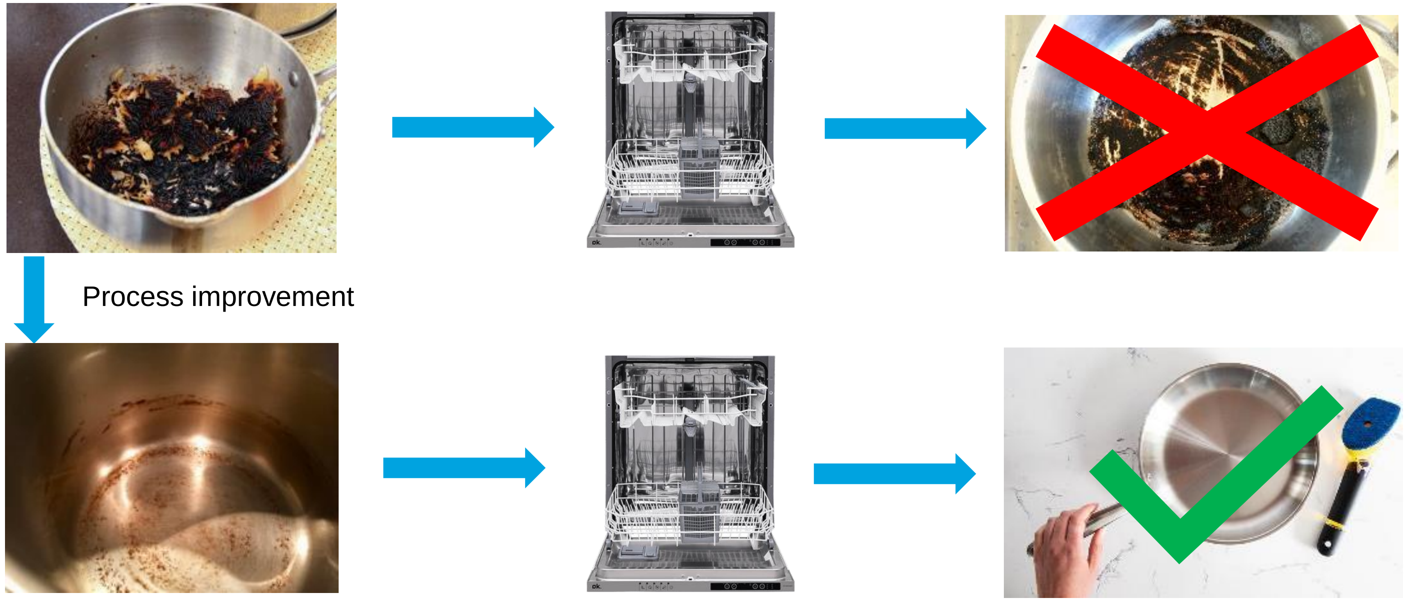
=Selecting a good dish washer

Qualify CSP performance by doing tests with standardized contaminated parts

Step 2: Product release

=Making sure the dishes always come out clean

Make sure the delivered parts are in such a state that they can be cleaned to grade 1



Note: for both steps we must be able to prove that the parts are clean, so CSP must be able to qualify parts

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Critical part particle cleanliness measurement

Particle Measurement Card (PMC) FastMicro methodology

Using only visual inspection, you only see particles down to ~50 µm

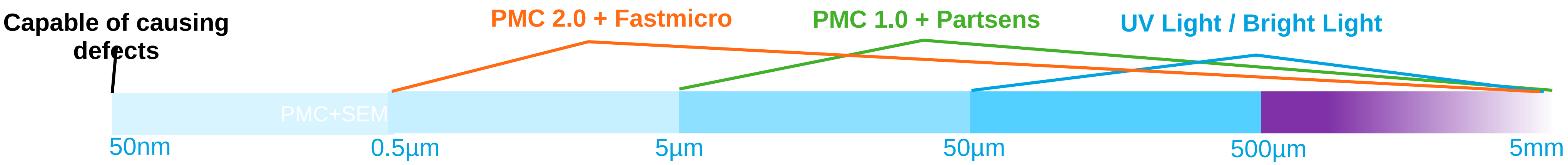
Particles in the range of tens of nms can already cause defects

This is what drove the development of PMC + FastMicro

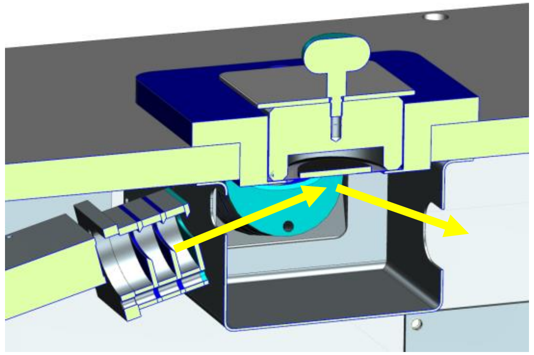
The 0.5 µm sensitivity is sufficient to judge risks @ tens of nms for wafer and reticle defectivity

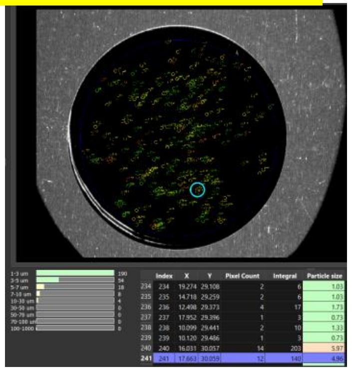
UVA black light inspection lamp

Bright light inspection lamp



BPMC sampling followed by FastMicro measurement





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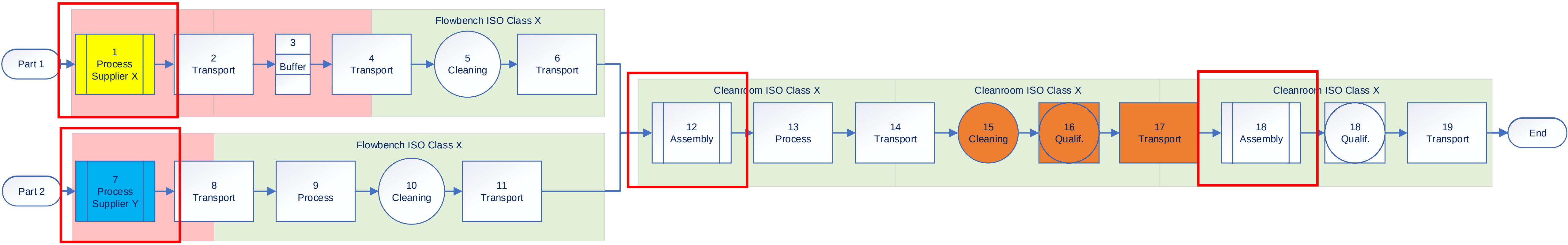
- Defectivity within ASML
- Critical defect size
- **Contamination control approach (product lifecycle and defectivity chain)**
  - by Design
  - **by Manufacturing**
    - Clean parts strategy
    - Surface cleanliness – particles measurement
    - **M-flow control**
- Examples how manufacturing and machining processes contribute to defectivity
- Summary and conclusions

M-Flow control

Review and release the manufacturing steps of critical parts – secure stable manufacturing



1 Identify the main manufacturing steps involved on product realization

2 Add information about the environment where each step occurs

3 Use different colors to indicate the n-Tiers

4 Critical process (cleaning, assembly, process at n-Tier) must have additional MFlow

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Some examples (build clean)

Cleanroom environment

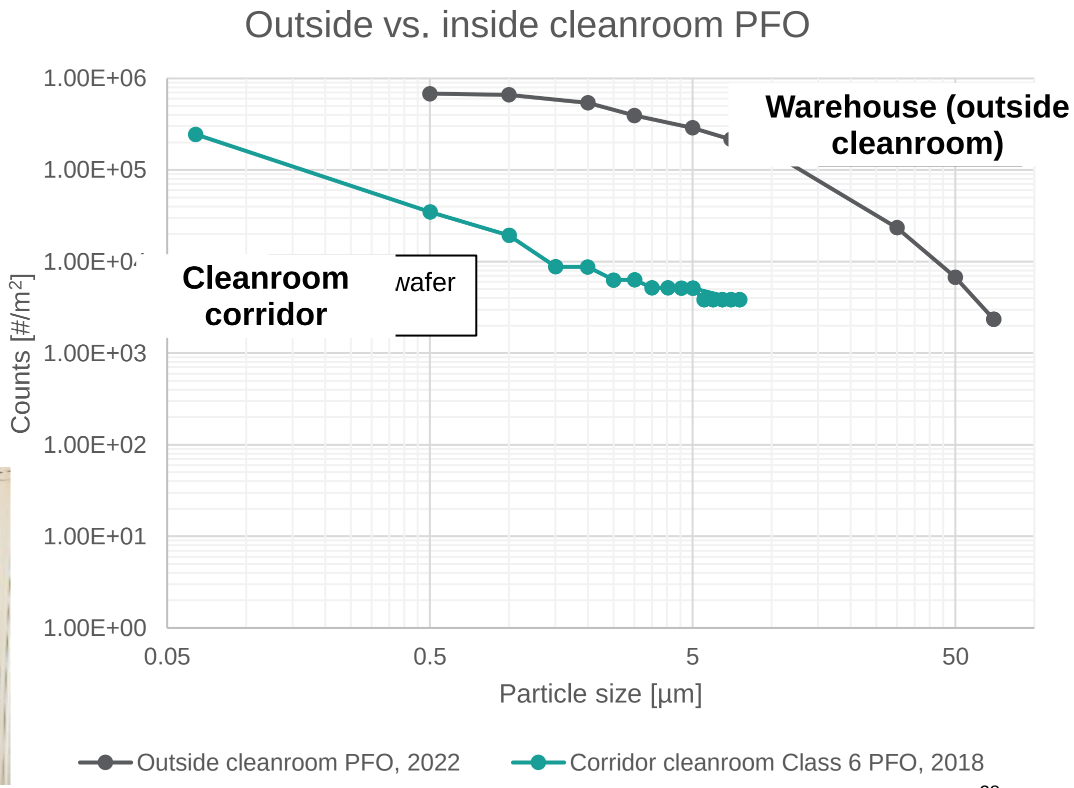
Why is this a risk?

Contamination levels outside a cleanroom environment are substantially higher than in a cleanroom adding particle contamination

Possible solutions:

Perform critical activities in a cleanroom

Clean parts before entering a cleanroom, after cleaning double bag. Remove first layer on entering cleanroom



Some examples (build clean)

Bolting

Why is this a risk?

Bolting and unbolting causes substantial amount of particles

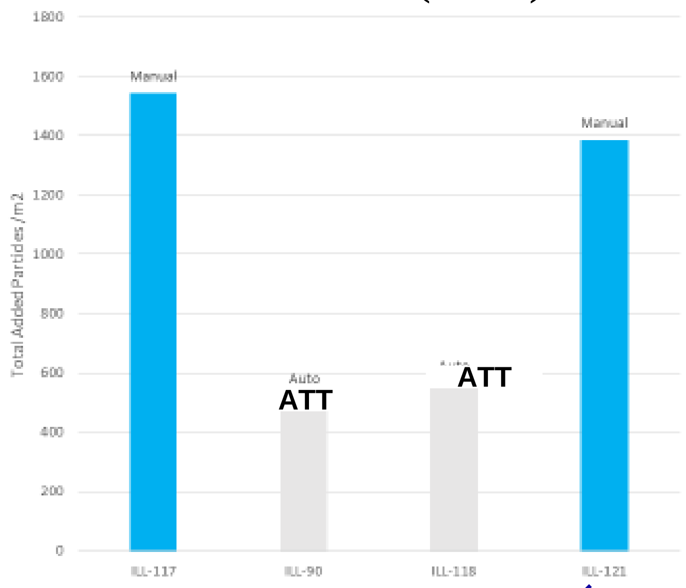
Possible solutions:

Automated bolting reduces particle generation

Clean after bolting activity

Cover / shield critical surfaces during bolting activities

Particle Fall Out (PFO) #/m^2



ATT

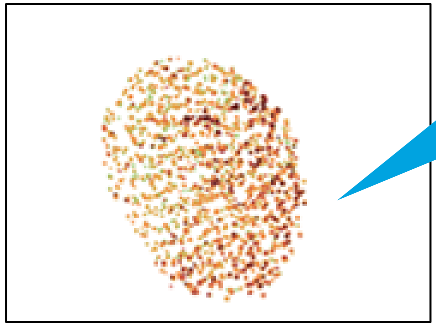
Manual tool

Some examples (build clean)

Cleanroom Gloves

Why is this a risk?

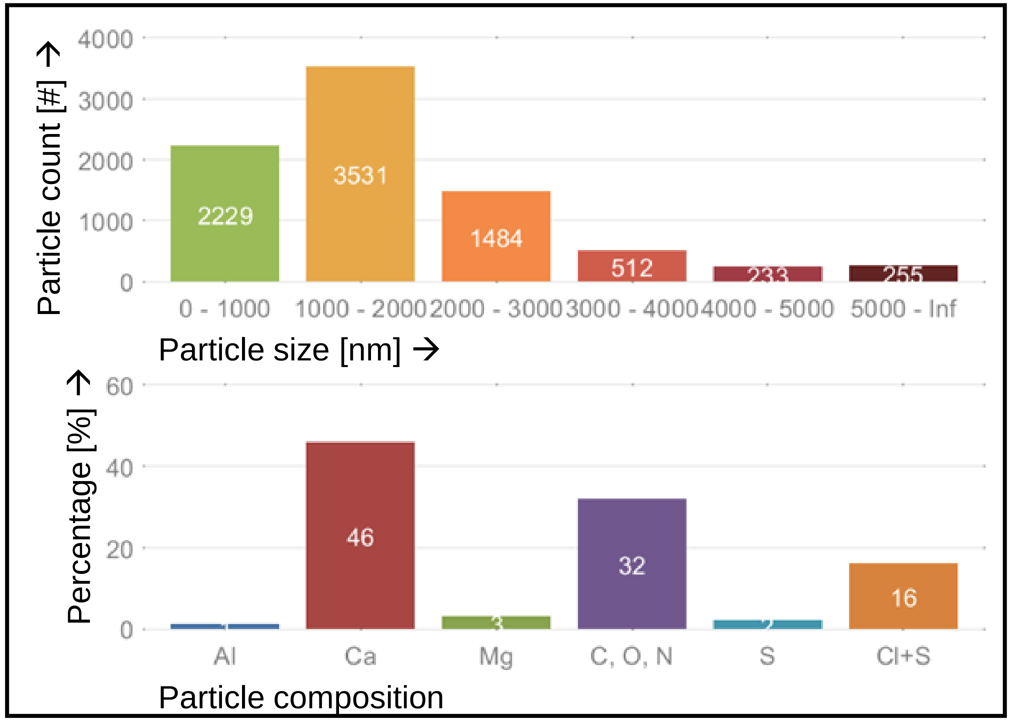
Contacting critical clean surfaces, even with cleanroom gloves, can cause unacceptable cross contamination



Print on wafer from a NXE cleanroom glove (straight from packaging)

2E6 particles ≥ 5μm /m^2

1 single contact: >8000# ≥40nm



Possible solutions:

Define and use handling area's for critical parts on less critical surfaces

Use tooling for handling

Implement cleaning step if contacting (with tooling) cannot be avoided

Some examples (m-flow control)

Wire EDM

Why is this a risk?

The process leaves a recast layer

This recast layer is brittle = particle risk

Recast layer also contains wire material

In many cases, Cu/Zn is used

Zn = HIO element

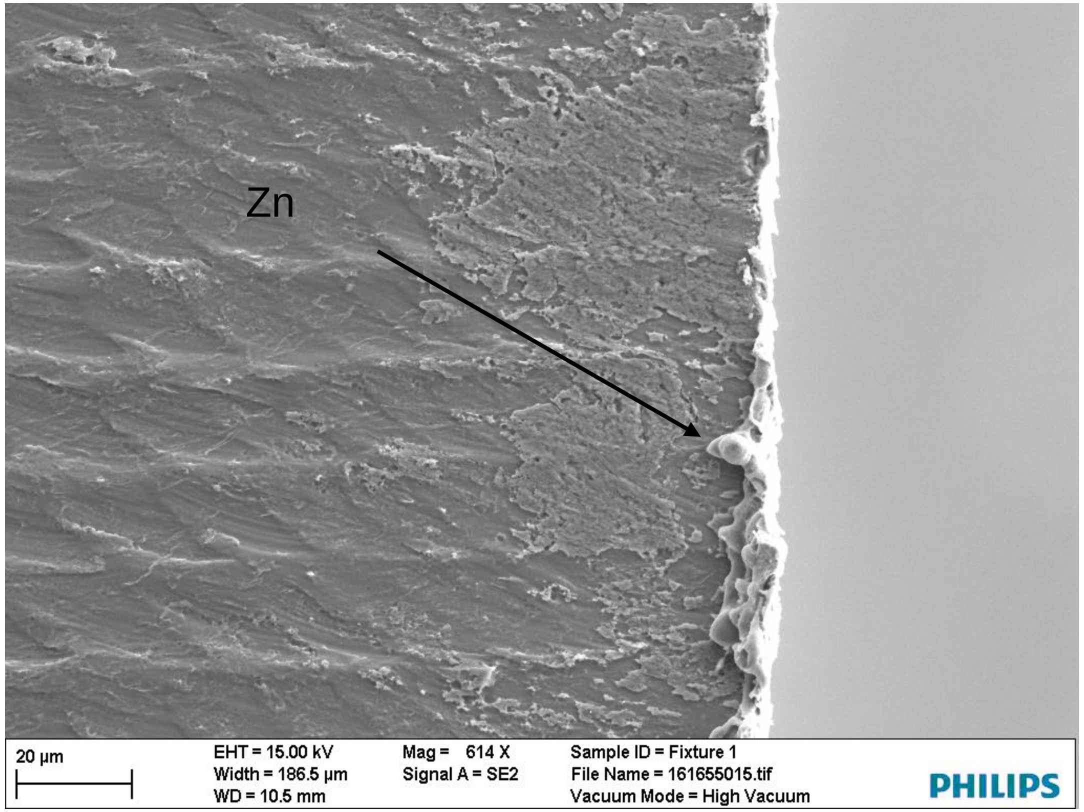
Ultrasonic cleaning is not a solution

Possible solutions:

Use other wire material (Mo, W)

Post-milling to remove recast layer

Extended pickling



Some examples (m-flow control)

Grit blasting

Why is this a risk?

In some cases a rough surface is needed

Surface is made rough by grit blasting

AlO_x particles are embedded in the surface

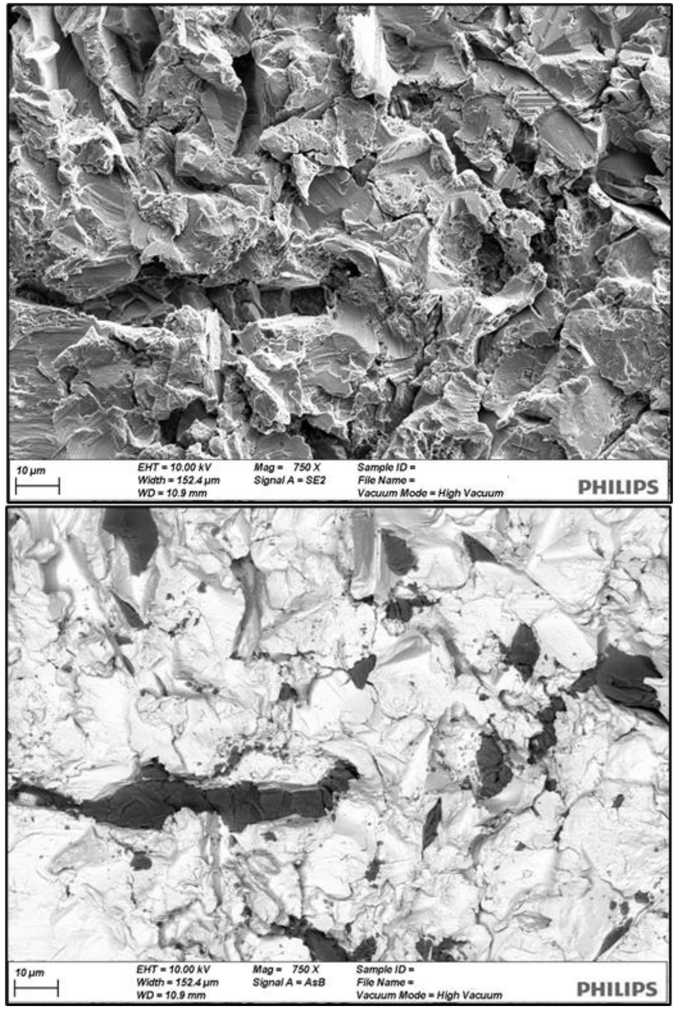
These are not removed by ultrasonic cleaning…

…but under EUV conditions they are released

Possible solutions:

Avoid grit blasting for particles grade 1!

Use other process to create roughness



Some examples (m-flow control)

Laser engraving

Why is this a risk?

Laser locally melts material, causing droplets

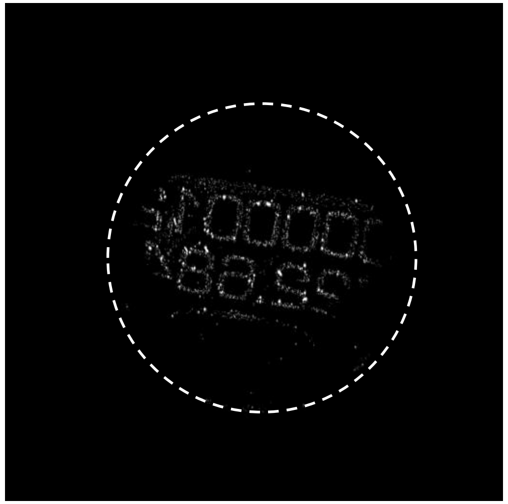
This can cause a high amount of particles

Wipe cleaning will not remove these particles

Possible solutions:

Perform engraving earlier in the process

Use laser annealing to make serial number?



Unless you want to be able to read serial numbers with PMC…

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Summary and conclusions

- Product yield and therefore contamination control is key in the semiconductor industry
- Particle contamination control within ASML mainly focusses on wafer and reticle defectivity
- Defectivity is not tangible given the size of particles being critical for contamination control
- ASML considers the full product lifecycle and aims to fully understand the defectivity chain for a successful contamination control approach
- For critical parts a cleaning approach and m-flow control is in place to assure defectivity performance
- Monitoring capability for particle contamination is available
- Several examples show the critically of manufacturing for contamination control
- Awareness and knowledge on contamination control in the ASML supply chain is critical for ASML's and ASML's customer success in providing high product yield

Knowledge Sharing Centre

Thank you for your attention

Knowledge Sharing Centre